IN THE SPECIFICATION

Please amend the paragraph beginning at column 2, line 11 as follows:

The clock regenerating circuit 75 regenerates A/D conversion clocks, of which the timing at which the [A/ID] A/D converters 72 and 73 execute an A/D conversion (the so-called eye pattern in fully open state) matches the phase, from a received signal to be detected by the orthogonal detecting unit 75 and then supplies them respectively to the A/D converters 72 and 73. The clock regenerating circuit 75 is formed of a square detecting unit 76, a filer 77, and a PLL circuit 78. The PLL circuit 78 is formed of a phase detector (PD) 79, a loop filter 80, an amplifier 81 and an oscillating unit 82.

Please amend the paragraph beginning at column 2, line 45 as follows:

The clock regenerating circuit 83 proposed by Japanese Patent Laid-open Publication (Tokukaisyo) No. 63-215235 as shown in FIG. 61, is formed of a phase deviation detection unit 831, [a] an infinite phase shifter 832, and an oscillating unit 833. Numeral 81 represents a demodulating unit which demodulates a received signal and 82 represents a data regenerating unit that regenerates a demodulated signal (data) from the demodulating unit. The data regenerating unit 82 consists of an equalizer (EQL) 821 that subjects a demodulated signal to an equalizing process and an identifier (A/D converter) that identifies and encodes (digitalizes) the level of the demodulated signal processed by the equalizer.

Please amend the paragraph beginning at column 4, line 13 as follows:

According to the present invention, the clock regenerating circuit arranged in a receiving unit of multiplex radio equipment, the receiving unit including an identifying unit for identifying

a signal at a predetermined identification level, the signal being obtained by demodulating a multi-level orthogonal modulated signal and an equalizing circuit for subjecting the demodulated signal to an equalizing process, the clock regenerating circuit regenerating a signal identification clock for the identifying circuit an then supplying the signal identification clock to the identifying circuit[;], is characterized by a clock regenerating unit for regenerating the signal identification clock based on a signal before the multilevel orthogonal modulated signal is detected[;], a phase adjusting unit for adjusting the phase of a clock from the clock regenerating unit and then supplying the phase-adjusted clock to the identifying circuit[;], and a clockphase detecting unit for detecting a phase component of the signal identification clock based on input/output signals of the equalizing circuit and then supplying the result as the phase adjustment control signal to the phase adjusting unit.

Please amend the paragraph beginning at column 4, line 50 as follows:

Furthermore, according to the present invention, the clock regenerating circuit arranged in a receiving unit of multiplex radio equipment, the receiving unit including an identifying circuit for identifying a signal at a predetermined identification level, the signal being obtained by demodulating a multilevel orthogonal modulating signal and an equalizing circuit for subjecting the demodulated signal to an equalizing process, the clock regenerating circuit regenerating a signal identification clock for the identifying circuit and then supplying the signal identification clock to the identifying circuit[;], is characterized by a clock phase detecting unit for detecting a phase component of the signal identification clock based on [input/output] <u>input/output</u> signals of the equalizing circuit[;], a loop filter unit for integrating the output from the clock phase detecting unit[;], and an oscillating unit for producing a signal identification

clock for the identifying circuit to the identifying circuit, in response to as a control input the output from the loop filter unit.

Please amend the paragraph beginning at column 6, line 6 as follows:

According to the present invention, the clock regenerating circuit arranged in a receiving unit of multiplex radio equipment, the receiving unit including an identifying circuit for identifying a signal at a predetermined identification level, the signal being obtained by demodulating a multilevel orthogonal modulated signal, the clock regenerating circuit regenerating a signal identification clock for the identifying circuit and then supplying the signal identification clock to the identifying circuit[;], is characterized by a clock phase detecting circuit for detecting a phase component of the signal identification clock based on clock phase difference information supplied to the identifying circuit and signal error differential information obtained by the identifying circuit which supplies it to the clock regenerating circuit[;], a loop filter unit for integrating the output from the clock phase detecting unit[;], and an oscillating circuit for producing a signal identification clock for the identifying circuit to the identifying circuit, in response to the output as a control input from the loop filter circuit.

Please amend the paragraph beginning at column 13, line 66 as follows:

In the clock regenerating circuit 2A, the identifying circuit 11 may be formed of plural identifying units corresponding to the number of plural signals obtained by demodulating the multilevel orthogonal modulated signal. The clock regenerating unit 15, the phase adjusting unit 16, and the clock phase detecting unit [14] 14A may be used in common to plural identifying units.

Please amend the paragraph beginning at column 25, line 50 as follows:

In the clock regenerating circuit 35A having the above-mentioned configuration, like the configuration shown in FIGS. 7 and 9, the phase component detecting unit 26A arranged corresponding to the channel (Ich) identifying unit 23 detects the phase shift of and A/D conversion clock based on an Ich signal while the phase component detecting unit 26B arranged corresponding to the channel (Qch) identifying unit 24 detects the phase shift of an A/D conversion clock based on a Qch signal. The integrator [27] 27A averages the phase shift of an A/D conversion clock to supply as a phase adjustment and control signal for the phase shifter 28A to the phase shifter 28A while the integrator [27] 27B averages the phase shift of an [A/ID] A/D conversion clock to supply as a phase adjustment and control signal for the phase shifter 28B to the phase shifter 28B. As a result, the phase shifters 28A and 28B adjust independently the phase of the A/D conversion clock regenerated in the clock regenerating unit 29 and supply it respectively to the identifying units 23 and 34.

Please amend the paragraph beginning at column 26, line 38 as follows:

In the inclination judging unit 30A having the above-mentioned configuration, the FF circuit 306, for example, as shown in FIG. 16, latches the current Ich signal (at the time"0") and the past Ich signal (at the time "-T/2") delayed by the time T/s by the [FE] FF circuit 305 and then outputs them to the comparing unit 307 according to the basic clocks from the frequency divider 36.

Please amend the paragraph beginning at column 34, line 53 as follows:

Hence the phase shift of an [A/ID] A/D conversion clock for the A/D converters 23A, 23B, and 24 can be adjusted automatically and with high accuracy to supply to the identifying units (A/D converters) 23A, 23B, and 24.